**Architecture Quiz Questions and Answers**

**Chapter 6**

1. Someone give you an arbitrary line of assembly language code and on that line there is one and only one instruction. Which of the following is true about the number of bits that that instruction will take after it is converted to machine language?
   1. A – it will take up a definite, fix number of bits, which will depend on the architecture of the system (for example, in MIPS, it would be 32 bits)
2. Someone give you an arbitrary line of assembly language code and on that line there is one and only one instruction (not a pseudo-instruction). That instruction refers to a particular register as the destination of the operation which it indicates. Which of the following is true about how the choice of which register is represented after the instruction is converted to machine language?
   1. B – The choice of which register is encoded in a specific range of bits within the machine language representation of the instruction
3. Someone give you an arbitrary line of assembly language code and on that line there is one and only one instruction (not a pseudo-instruction). That instruction refers to a particular register as a possibility where the execution might need to transition to depending on other factors. Which of the following is true about how the target address is represented after the instruction is converted to machine language?
   1. C – The target address (or a subsequence of it, or the difference between it and the address of the current instruction, or a subsequence of that) is, in machine language, represented by a specific range of bits within the machine language
4. You’re designing an assembly language You find you have many instructions that do something like “result = operand1 OPERATION operand2”. You’re already decided that “result”, “operand1”, and “operand2” will be registers. Which of the following seems like a reasonable way to encode these types of instructions in the machine language?
   1. D – For all instructions of this type, some vary based on the operation
5. Someone give you an arbitrary single line of assembly language code, and on that line there is one and only one instruction (not a pseudo-instruction). That instruction has a particular immediate value. Which of the following is true about how the immediate value is represented after the instruction is converted to assembly language?
   1. A – The immediate value is converted to binary and (if it fits) it is placed within the range of bits specified for it. (If it doesn’t fit , then this is a syntax error)
6. An instruction refers to the value in a register. Which of the following is the addressing mode when that happens?
   1. A - Register
7. An instruction refers to a \_\_\_\_\_\_\_\_\_ Which of the following is the most likely addressing mode in MIPS when that happens?
   1. B - Immediate
8. An instruction refers to a target address. Which of the following is the most likely addressing mode in MIPS when that happens?
   1. C – PC-Relative
9. [Need to know] An instruction refers to a value found at an address that is calculated by adding an immediate to the value in a register. Which of the following is a name for that type of addressing mode?
   1. D - base
10. Not true..?? You’re writing an assembly language program that loads date from somewhere within the an array Which of the following is NOT true?
    1. D – Fourth, you then write your value to the address you calculated
11. You’re writing an assembly language program that reads data from somewhere within an array. Which of the following is true?
    1. D – You load the value from the address you calculated
12. [KNOW] You’re writing a loop in assembly language. What sort of instructions do you use to keep on looping?
    1. C – An instruction that sets the program counter to a location that has already been executed
13. You’re writing a loop in assembly language. You need to know when to keep on looping, and when to stop looping. What sort of instruction do you use to determine this?
    1. B – An instruction that conditionally affects the program counter.
14. In MIPS, each instruction is 32 bits. This means that the next instruction, after the current instruction, is how many bytes away from the current instruction?
    1. D-4
15. In a typical MIPS map, there is a place where globals and static data (such as its constants) are stored. This is different from the place where function code is stored within a particular range of memory addresses, started at one end and grouwing towards the other end. Given a list of functions and the number of machine language instructions that they take, how ould ou calculate what address each function should have?
    1. A – The first function starts at the first address within the range, and then after all of its instructions, then the next function begins, and so on.
16. Given job of writing new pseudo instruct. Which of the following are you careful NOT to do?
    1. A – Replicate the functionality of existing instruction for now obvious reason.
17. You’re given the job of writing new pseudo-instructions which of the following careful NOT to do?
    1. D – None of the above (write pseudo instructions that make sense as pseudo instructions, avoid using pseudo-instructions to implement pseudo-instructions, and write pseudo instructions what use as few instructions as possible for efficiency)
18. A pseudo-instruction requires an immediate that is greater in size than any of the immediate fields that any of your instructions support. What do you do?
    1. A – Load half of the immediate into the assembler temporary, and then load the other half, and then continue.
19. How many bits does it take to indicate the maximum amount possible that you might want to shift a 32 bit value in one particular direction? (want to do 31 or less bits)
    1. C - 5

**Chapter 7**

1. In order to make a prog. Execute faster, which of the following do we need to INCREASE? (# inst \*sec/cycle \*cycles/instruction)
   1. D – instructions per cycle
2. Compared to a single-cycle MIPS implementation, what does the multi-cycle MIPS implementation INCREASE?
   1. B – cycles per instruction
3. For a multi-cycle implementation If there were 4 instructions Types, and they took 1, 2, 3, and 4 cycles each respectively, ad their frequency of use within a program was 10%, 20%, 30% 40% each respectively, then which of the following is closest to the avg. CPI? (1\*.1 + 2\*.2+3\*
   1. C - 3
4. [KNOW- but only conceptually] For a pipelined processor that has 20% of jumps, 40% branches, 20% loads that are used by the next instruction, and 20% all other instructions, and all jumps and branches cause the net instruction to be flushed, what would the avg CPI be (assuming no other hazards)? (remember, for pipeline processors, when everything is going good the CIP is 1. In these cases, if not good, then 2). (.2\*2 + .4\*2+.2\*2 + .2\*1 = 1.8)
   1. D - 1.8
5. For a pipelined processor that has 20% of jumps, 40% branches, 20% loads that are used by the next instruction, and 20% all other instructions. Jumps cause the next isntr. To be flushed, and half of all branches are mis-predicted, what would the avg CPI be (assuming no other hazards) ? (Remember for pipelines processors, when everything is going good, the CPI is 1. In these cases, if not good, then 2). [.2\*2 + .2\*2+.2\*1 +.2\*2+.2\*1]
   1. C – 1.6
6. When figuring out the CPI for a segment of code that involves a loop, which of the following do you do?
   1. B – count the instructions executed (need to do more, but need to do this step)
7. When figuring out the CPI for a segment of code that involves a loop, which of the following do you do?
   1. A – determine how many times the loop repeats
8. For a segment of code that involves one and only one loop: if the only condition. To break of a loop is somewhere in the body of the loop (not in last instruct), then which of the following is is true for any execution of this segment of the code?
   1. A – The instruction immediately before the conditional will be executes one more than the instruction immediately after the conditional
9. When figuring out the CPI for a segment of t code that involves a loop, which of the following do you do?
   1. A- For every instruction, figure out the number of cycles that that instruction takes.
10. When figuring out the CPI for a segment of code that involves a loop, which of the following do you do?
    1. A – Multiply the number of cycles that the loop body take by the number of times the loop body is executed
11. When figuring out the CPI for a segment of code that involves a loop, which do you do?
    1. C – Remember the instruction both before and after the loop
12. When calculating the CPI, you divide the tot. number of cycles by the number of
    1. A- instructions executed
13. Which of the following is not a type of hazard covered in this chapter?
    1. C - Duke
14. If we increase the rate at which we correctly predict our branches, how does this reduce our CPI?
    1. D – all of the above (– It causes the avg CPI of the branches to be reduces likelihood of stalling, and C)
15. A pipelined MIPS processor is running, which of the following program. Which of the possible statements is true and relevant?

*lw $t0 0($0)*

*addi $t1, $t0, 1*

* 1. C – there is a data hazard (unless we have data forwarding)

1. A pipelined MIPS processor is running, which of the following program. Which of the possible statements is true and relevant?

*beq $t0, $t1, else*

*else:*

*Beq $t2, $t3, done*

*beyond:*

*Addi $t4, $t5, 1*

*done:*

* 1. B – there are control hazards

1. A pipelined MIPS processor is running, the following program. Which of the possible statements is true and relevant?

*lw $t0, 0($0)*

*addi $t1, $t2, 3*

* 1. D – there are no hazards

1. What is the CPI of a program that has zero instructions?
   1. Both C – Undefined and D – cannot determine because cannot divide by 0
2. In which of the following is the CPI always 1?
   1. A – single-cycle implementation
3. With superscalar(means multiple copies of the pipeline), out-of-order, and register renaming, the goal is to increase which of the following?
   1. A – instruction level parallelism
4. If a program has one instruction, and we are on a single-cycle implementation of the MIPs processor, which of the following CPI of the program?
   1. A - 1
5. [KNOW] If a program has one instruction, and we are on a pipelined implementation of the MIPS processor, which of the following CPI of the program?
   1. E – none of the above (should be how many stages are in the pipeline)
6. On a single cycle implementation of the MIPS processor, if we have a program that take 100 instructions to complete, how make cycles does it take?
   1. A -100

**Chapter 8**

1. If we have a fixed cost and we increase the speed, what happens to the size?
   1. B – it decreases
2. If we have a fixed cost and we increase the speed, what happens to the size?
   1. It decreases
3. If we have a fixed speed and we decrease the cost, what happens to the size?
   1. B- it decreases
4. If we have a fixed size and we increase the cost, what happens to the size?
   1. A- increases
5. If we have a fixed size and we increase the cost, what happens to the size?
   1. A- it increases
6. ??
   1. Q
7. If everything else remains the same, and the miss rate increases, what happens to the program execution time?
   1. B- it decreases
8. If everything else remains the same, and hit rate increases
   1. A -increases
9. If everything else remains the same, and hit rate decreases
   1. B-decreases
10. IF the capacity and associativity of a cache remain the same, and the size of a block increases, what happens the the number of blocks?
    1. ksldf
11. [Know capacity and blocksize] If the capacity and associativity of a cache \_\_\_\_\_\_\_\_\_\_, and the size of a block \_\_\_\_\_, what happens to \_\_\_\_\_\_\_\_?
    1. A -increases
12. If the capacity and associativity of a cache remain the same, and the size of a block increases, what happens to the number of blocks?
    1. C – stays the same
13. #14 If the capacity and associativity of a cache \_\_\_\_\_\_\_\_\_\_, and the size of a block \_\_\_\_\_, what happens to \_\_\_\_\_\_\_\_?
14. #15 If the capacity and associativity of a cache \_\_\_\_\_\_\_\_\_\_, and the size of a block \_\_\_\_\_, what happens to \_\_\_\_\_\_\_\_?
    1. A-increases
15. If the capacity and associativity of a cache \_\_\_\_\_\_\_\_\_\_, and the size of a block \_\_\_\_\_, what happens to \_\_\_\_\_\_\_\_?
    1. Decreases
16. #17 Will not ask I
    1. Q
17. If the size of a pages stays the same, but the number of virtual address bits increases, what happens to the number of virtual pages?
    1. -decreases
18. If the size of a page stays the same, but the number physical address bits decreases, what happens to the number of physical pages?
    1. B- decreases
19. If the size of a page stays the same, but the number physical address bits increases, what happens to the number of physical pages?
    1. A- increases
20. Using a page table adds overhead to each memory access. This memory access overhead can be reduced by caching the page table lookups. This page table lookup cache is commonly called a
    1. E- none of above (TLB)
21. When an instance of program is running, it is called a process. Each process has its own page table. This means that each process has its own page table. This means that each process has virtual addresses that (unless shared memory is used) map to different physical addresses. This feature increases:
    1. B – security (cannot dual-write stuff)
22. #25If the miss rate and hit rate stay the same, but the cache access time increases, what happens to avg. memory access time?
    1. A – it increases
23. If the miss rate and hit rate stay the same, but the cache access time decreases, what happens to the average memory access time?
    1. B – decreases
24. If there is an attempt to access memory that has not been accessed before, the way in which we determine that this is the case, rather than just providing whatever garbage happened to be in the cache, is through the use of:
    1. C –both of the above: tag bits and a valid bit